REMARKS

Claims 1, 2-17, 19-21, 23 and 24 are pending in the application. Claims 1, 2-17, 19-21, 23 and 24 stand rejected under 35 U.S.C. 103(a) as being unpatentable over cited portions of U.S. Patent No. 5,826,096 (hereinafter, Baxter) in view of cited portions of "Structured Computer Organization," by Andrew S. Tanenbaum (Prentice-Hall 1976) (hereinafter, Tanenbaum). Applicants respectfully traverse this rejection, hereby and as set forth below.

Regarding independent claim 1, Baxter and Tanenbaum do not disclose or suggest, alone or in combination, a processor including "a functional unit...that executes an instruction that operates upon plural registers of [a] register file, including at least one register explicitly identified by an explicitly defined register specifier and at least one other register implicitly identified by the explicitly-defined register specifier" as required by independent claim 1. For example, although Tanenbaum discloses the use of an index register to implement autoindexing, said index register being incremented after an initial execution of an instruction, and upon each subsequent execution of the instruction, Baxter and Tanenbaum do not disclose or suggest, alone or in combination, "an instruction that operates upon plural registers" wherein said instruction operates upon "at least one register explicitly identified by an explicitly defined register specifier and at least one other register implicitly identified by the explicitly-defined register specifier" (e.g., each time it is executed). On the contrary, Tanenbaum teaches conventional incrementation of a pointer upon subsequent executions of an instruction. Therefore, independent claim 1 is allowable over Baxter and Tanenbaum for at least this reason. Dependent claims 2-17 and 19 depend from claim 1 and are allowable for at least this reason.

Regarding independent claim 20, Baxter and Tanenbaum do not disclose or suggest, alone or in combination, a method of operating a processor including "explicitly defining a register specifier of a register operated upon during executing of an instruction," and "implicitly deriving a register specifier of at least one other register operated upon during executing of the instruction based on the explicitly defined register specifier," all as required by independent claim 20. For example, although Tanenbaum discloses the use of an index register to implement autoindexing, said index register being incremented after an initial execution of an instruction, and upon each subsequent execution of the instruction, Baxter and Tanenbaum do not disclose or

suggest, alone or in combination, "explicitly defining a register specifier of a register operated upon *during executing of an instruction*," and "implicitly deriving a register specifier of at least one other register operated upon *during executing of the instruction* based on the explicitly defined register specifier," (e.g., both steps occurring during an execution of the instruction). On the contrary, Tanenbaum teaches autoindexing between subsequent executions of an instruction. Therefore, independent claim 20 is allowable over Baxter and Tanenbaum for at least this reason. Dependent claims 21 and 24 depend from claim 20 and are allowable for at least this reason.

In view of the amendments and remarks set forth herein, the application and claims therein are believed to be in condition for allowance and a notice to that effect is solicited. Nonetheless, should any issues remain that might be amenable to resolution through a telephonic interview, the Examiner is requested to telephone the undersigned.

CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office on the date shown below.

Michael P. Noonan — March 31, 2003 (Date)

Respectfully submitted,

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